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09/870,458	06/01/2001	Joshua M. Conner	068354.1439	8446

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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/870,458	CONNER ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 19-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Marui et al., US Patent 5,559,730 (herein after referred to as Marui).

3. Referring to claim 19, Marui has taught a method implemented in a computer system, of shifting a multiword value comprising:

a. performing a first shift operation on a first portion of the multi-word value to produce one or more overflow bits (Figure 5-7, column 7, line 55-column 10, line 28, Step 2-2 and Step 102-2);

b. performing a second shift operation on a second portion of the multi-word value (Figures 5 and 6, column 7, line 51-column 9, line 33, Steps 3-2 and 3-3, ad Steps 103-2 and 103-3), where the second shift operation comprises:

i. producing a shift result (Figure 5-7, column 7, line 55-column 10, line 28, Step 3-2 and Step 103-2, intermediate data D); and

ii. concatenating the shift result and the overflow bits (Figure 5-7, column 7, line 55-column 10, line 28, Step 3-3 and Step 103-3, OR operation); and

iii. where the second shift operation is a multi-precision shift instruction (column 7, lines 51-54, column 8, lines 24-29, column 9, lines 5-20 and lines 34-46) and where the first shift operation and second shift operation are performed sequentially (Figure 5-7, column 7, line 55-column 10, line 28, The first shift operation produces the overflow bits in Register 40 and then the second shift operation is performed sequentially after the first shift operation such that the first shift operation must complete before the second shift operation completes so that the data in register 40 is available to the second shift operation.) and further where the one or more overflow bits are stored in an overflow register prior to concatenation with the shift result (Figure 5-7, column 7, line 55-column 10, line 28, Step 3-2 and Step 103-2, Register 40).

4. Referring to claim 20, Marui has taught the method of claim 19, as described above, and further comprising:

a. fetching and decoding the multi-precision shift instruction (Figure 3, Shift operations are necessarily fetched and decoded to carry out the multi-precision shift operations. Figure 3, element 307, Figures 5 and 6, column 7, line 51-column 9, line 33); and

b. outputting the result (Figures 5 and 6, column 7, line 51-column 9, line 33, result is output to registers 70 and 71).

5. Referring to claim 21, Marui has taught the method of claim 20, as described above, and where the multi-precision shift instruction is a shift left instruction (Figure 5, column 7, lines 64-67).

6. Referring to claim 22, Marui has taught the method of claim 20, as described above, and where the multi-precision shift instruction is a shift right instruction (Figure 6, column 8, lines 43-47).

7. Referring to claim 23, Marui has taught the method of claim 20, as described above and where the multi-precision shift instruction specifies a shift increment (Figures 5 and 6, column 7, line 51-column 9, line 33, N is the specified shift increment which is stored in register 10.).

8. Referring to claim 24, Marui has taught the method of claim 23, as described above, and where the shift increment is greater than or equal to the number of bits in a word (column 7, line 55-67, N is an integer equal to or more than 1, so when N=16 then the shift increment is equal to the number of bits in a word.).

9. Referring to claim 25, Marui has taught the method according to claim 23, as described above, and where the shift increment is less than the number of bits in a word (column 8, lines 34-37, When N is equal to 1.).

10. Referring to claim 26, Marui has taught the method of claim 19, as described above, and further comprising:

a. storing one or more bits shifted out of the second portion of the multi-word value during the second shift instruction in a carry register (Figure 7, Register 40 from the intermediate data register 71, step 103-4).

11. Referring to claim 27, Marui has taught the method of claim 19, as described above, and where concatenating the shift result and the overflow bits comprises:

a. performing a logical OR operation on at least one bit in the shift result and at least one overflow bit (Figures 5 and 6, column 7, line 51-column 9, line 33, Step 3-3, OR operation).

12. Referring to claim 28, Marui has taught the method of claim 19, as described above, and further comprising:

a. storing one or more of the overflow bits in a carry register (Figures 5 and 6, column 7, line 51-column 9, line 33, register 40).

13. Referring to claim 29, Marui has taught a processor for processing multi-precision shift instructions, comprising:

a. a program memory for storing instructions including at least one multi-precision shift instruction (column 5, lines 39-41, column 8, lines 24-29, column 9, lines 5-9, column 10, lines 11-16, The program to be executed is inherently stored in a program memory.);

b. a program counter for identifying current instructions for processing (column 5, lines 39-41, column 8, lines 24-29, column 9, lines 5-9, column 10, lines 11-16, This element is inherent in order to sequence through the instructions to execute the program.); and

c. a barrel shifter for executing shift instructions, including the at least one multiprecision shift instruction (Figure 5-7, column 7, line 55-column 10, line 28, shifter 20), the barrel shifter including:

i. one or more carry registers for storing values shifted out of sections of the barrel shifter (Figure 5-7, column 7, line 55-column 10, line 28, Register 40); and

ii. OR logic for concatenating values stored in one or more carry registers with values in the barrel shifter (Figure 5-7, column 7, line 55-column 10, line 28, Step 3-3, Step 103-3 and Step 104-3); and

d. where the barrel shifter is operable to shift a multi-word value (Figure 5-7, column 7, line 55-column 10, line 28, shifts a double or triple word value), and where when shifting a multi-word value the barrel shifter:

i. executes at least one shift instruction to:

(1) load a first operand into a section within the barrel shifter, where the first operand is a first portion of the multi-word value (Figure 5-7, column 7, line 55-column 10, line 28, LSP data is loaded into register 71 (figures 5 and 6) and register 72 (figure 7).); and

(2) generate one or more overflow bits and storing the one or more overflow bits in an overflow register (Figure 5-7, column 7, line 55-column 10, line 28, register 40 stores the overflow bits) and

ii. executes at least one multi-precision shift instruction fetched from the program memory to:

(1) load a second operand into a section within the barrel shifter, where the second operand is a second portion of the multi-word

value (Figure 5-7, column 7, line 55-column 10, line 28, MSP data is loaded into register 71 (figures 5 and 6) and intermediate data is loaded into register 72 (figure 7).);

(2) shift the second operand (Figure 5-7, column 7, line 55-column 10, line 28, step 3-2 and Step 103-2);

(3) concatenate the second operand with one or more of the overflow bits (Figure 5-7, column 7, line 55-column 10, line 28, Step 3-3 and Step 103-3 OR operation); and

(4) output the shifted value (The shifted value is output to register 71).

14. Referring to claim 30, Marui has taught the processor of claim 29, as described above, and where the multi-precision shift instruction is a shift left instruction (Figure 5, column 7, lines 64-67).

15. Referring to claim 31, Marui has taught the processor of claim 29, as described above, and where the multi-precision shift instruction is a shift right instruction (Figure 6, column 8, lines 43-47).

16. Referring to claim 32, Marui has taught the processor of claim 29, as described above, and where the multi-precision shift instruction is an arithmetic shift instruction (column 8, lines 29-34, column 9, lines 10-14).

17. Referring to claim 33, Marui has taught the processor of claim 29, as described above, and where the multi-precision shift instruction is a logical shift instruction (column 8, lines 29-34, column 9, lines 10-14).

18. Referring to claim 34, Marui has taught the processor of claim 29, as described above, and where the multi-precision shift instruction specifies a shift increment (Figures 5 and 6, column 7, line 51-column 9, line 33, N is the specified shift increment which is stored in register 10.).

Response to Arguments

19. Applicant's arguments with respect to claims 19-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

21. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571)

272-4170. The examiner can normally be reached on Monday-Friday with first Friday's off.

23. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

24. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TLM

Tonia L. Meonske
May 16, 2007